Dave Chandler...

Enclosed you will find the documentation available for the product Intellivoice. Wilson Quan will provide you with information on LUCKY, and Jim Becker will provide you with information for BIG MAC.

The enclosed information includes:

3330-5979	Intellivoice Product Engineering specification
3330-9259	Intellivoice Schematic
3330-9129	Intellivoice PCB Assembly
0086-0173	Buffer/Interface chip

Note that all this information is classified as CONFIDENTIAL. Any further information you require on Intellivoice you can get from me.

Regards,

Thom

Thom Randolph

cc: Bob DeCaro
Hugh Barnes

MATTEL ELECTRONICS

PRODUCT ASSURANCE SPECIFICATION

NUMBER 3330-5979	DATE 18Mar82
REVISION	DATE
PREPARED BY Thomas L. Randolph	DATE 18Mar82
SUBJECT 3330 Intellivoice Product Engineering Spec.	APPROVED BY / DATE

INTELLIVOICE
VOICE SYNTHESIS MODULE

3330 - 5979

PRODUCT ENGINEERING SPECIFICATION

REVISION SHEET

1.0 SUBJECT

1.1 Mattel Electronics 3330 Intellivoice Voice Synthesis module

2.0 INITIAL RELAESE:

Approved By:

Project Engineer Thomas C. Randolph

Manager, R & QA - Video Donald W. Bowe

Director, Product Assurance

Director, Systems Engineering Charles W. Ruder

3.0 REVISION APPROVAL

EDM #	DATE	SECTIONS AFFECTED	REVISION LEVEL	APPROVED BY
3330-61	MAY 6 1982		PR	See above

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(continued)

LIST OF FIGURES

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1 PURPOSE

This technical description of the 3330 electronic circuits will be from a functional and parametric standpoint only. No attempt will be made to include those parameters or functional details furnished in the variously appropriate component specifications.

Component tolerances shown here are for reference only, and the appropriate component specifications shall be used for all qualification of parts. All parts must adhere to their respective specification.

The technical description contained herein uses component reference designations as shown in the Intellivoice schematic, 3330-9259.

2 RELATED DOCUMENTS

Parts referenced with Mattel Electronics Part Numbers are supported by similarly numbered component specifications and/or drawings. All numbers are listed in the parts list, 3330-9991.

The 3330 should be assembled according to various specifications. These are:

INTELLIVOICE ASSEMBLY.....3330-9991
INTELLIVOICE PC BOARD ASSEMBLY...3330-9229

3 PRODUCT FUNCTION AND DESCRIPTION

3.1 PRODUCT DESCRIPTION

The 3330 produces audio speech signals when used in conjunction with a Master Component and/or Keyboard Component, and Voice Compatible game cartridges. Cartridges are deemed 'Voice Compatible' if they make use of the 3330 speech facilities. Cartridges which are not Voice compatible do not make use of the speech facilities, nor allow certain of the required speech production signal functions to be performed. Nonetheless, non-voice compatible game cartridges can be used with the 3330, but no voice game-play enhancement is provided.

When used in game-play, the Intellivoice unit 'speaks' through the sound channel of the television. It uses the same audio channel as the sound generator in the Master Component.

A volume control on the 3330 allows variance of the voice loudness level. This control does not affect the normal game sounds--only voice.

The 3330 unit will be the base for future peripherals. Additional hardware was included to provide for controlled communication between the Master Component and those peripherals. Future peripherals will plug into the top-mounted connector of the 3330.

3.2 CONNECTION

The 3330 plugs into the cartridge port of the Master/Keyboard component. The 3330 has a connector on its right-hand side for insertion of a game cartridge. On the top of the unit, under a plastic snap-in cover, the 3330 has a 'stacking connector', which is to be used with future peripherals in the Intellivision family. Refer to figure 1 for a view of the unit showing location of the three connectors, and their pin number orientations.

3.3 CONNECTOR PIN NUMBERING

Refer to figure 1 for a view of the unit showing the locations of the three connectors, and their pin numbering orientations.

Figure 1 also indicates the use of the connectors.

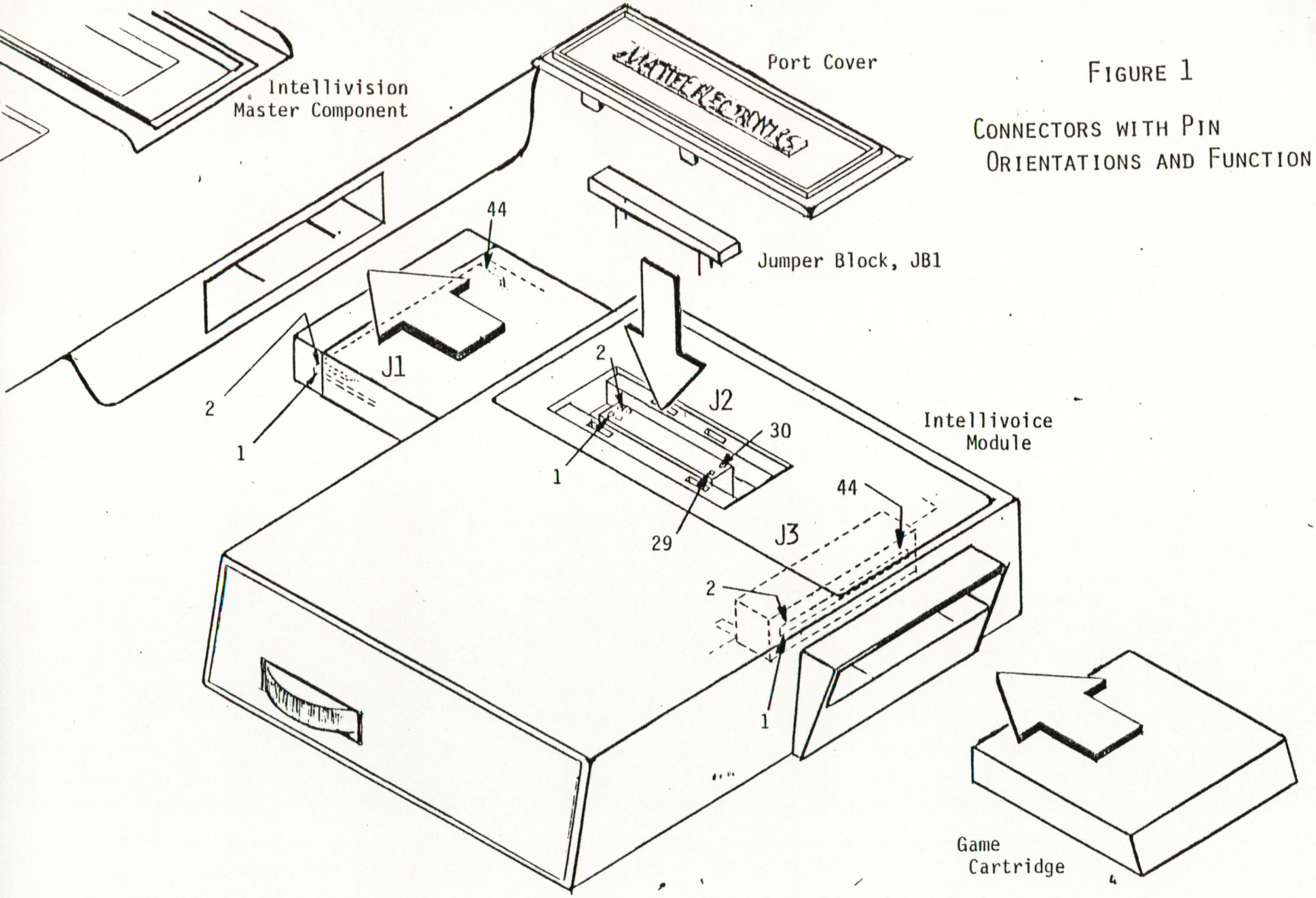


FIGURE 1

CONNECTORS WITH PIN ORIENTATIONS AND FUNCTION

3.4 PRODUCT FUNCTIONAL BREAKDOWN

The 3330 consists of a VLSI speech synthesizer, an LSI buffer/interface chip, an active audio filter/amplifier section, and provisions for current assistance to the Master/Keyboard component's +5V power supply.

Figure 2 shows a block diagram of the 3330. Refer to this diagram when reading the following sections discussing the various functional sections of the circuit.

3.4.1 SPEECH SYNTHESIZER

The speech synthesizer (Mattel Electronics Part Number 0086-0172) contains internal ROM encoded speech segments, referred to as 'Resident Code'. It also contains the actual synthesizer and controller logic, described in the specification for the chip.

3.4.2 BUFFER/INTERFACE CHIP

This chip, Mattel Electronics Part Number 0086-0173 contains the logic required to interface the speech synthesizer to the Master/Keyboard component cartridge bus.

Controlling input to the buffer/interface chip is primarily from the Master Component Microprocessor bus signals. Other controlling inputs are generated by the speech synthesizer during speech production.

The buffer has three means of transmitting data to the speech synthesizer and peripherals connected to the Stacking connector.

The first speech-oriented data transferrance method causes the synthesizer to produce speech segments contained in its internal ROM (Resident Code), and uses the peripheral data bus and associated handshake lines.

The speech buffer also contains facilities to allow the connection of peripherals through the top-mounted stacking connector. The stacking connector is normally protected by a snap-in cover and has a factory installed jumped block. The peripheral bus is used here to carry bi-directional microprocessor data, though with different handshake lines.

The second method of moving speech data allows the Master/Keyboard component to load custom speech data into the synthesizer. The data is changed with each different game cartridge used. It passes over the Voice serial bus, under control of the speech synthesizer, through a 640 bit FIFO array within the buffer/interface chip.

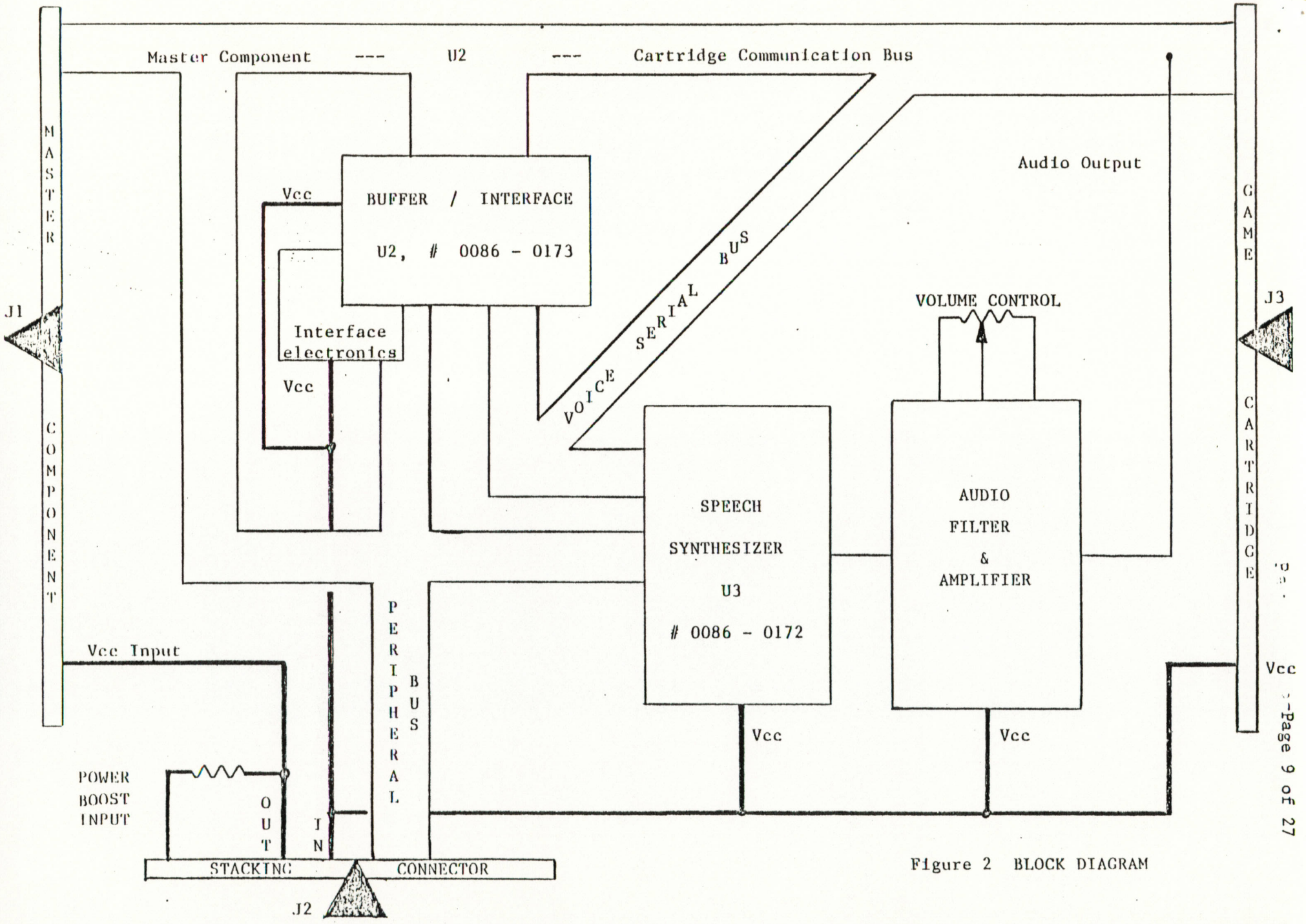


Figure 2 BLOCK DIAGRAM

3.4.3 AUDIO FILTER/AMPLIFIER

The audio filter changes the 40 KHz digital pulse-width modulated output of the speech synthesizer to an analog signal for output to the Master Component, with the frequency characteristics shown in figure 3. The spectral characteristics are described in detail in section 4.8.2.

The effective passband for the speech signals is from 150 Hz to 5 KHz. Within this is also a 3dB/Octave bass pre-emphasis.

Part of the filter is an adjustable-gain amplifier controlled by the volume control.

3.4.3.1 VOLUME CONTROL

The 3330 contains a front-mounted volume control. This control is used to adjust the output level of the unit so that it can be heard comfortably with the regular game sounds. The volume level is increased by rotating the knob to the right (counter-clockwise).

4 TECHNICAL DESCRIPTION

4.1 OVERVIEW

The 3330 functionally consists of a speech synthesizer (U3, #0086-0172), a buffer/interface chip (U2, #0086-0173), an audio filter/amplifier section, and a power supply boost provision. Refer to figure 2. This section gives detailed descriptions for all sections of the circuit. For more detailed information on the various chips and components, refer to their respective specifications.

4.2 CLOCK SIGNALS GENERATION

The speech synthesizer's clock is derived from a 3.12 MHz $\pm$ 1% ceramic resonator (Y1, #0089-0818). Y1 is connected across U3 pins 27 and 28 (also denoted by U2-27 and -28). Capacitors C1A and C1B (100pF $\pm$ 10% each, #0086-0705) and are added to increase the stability of the oscillator circuit. The clock frequency should be within 1% of the nominal value for acceptance. The resonator can be checked by using an oscilloscope and viewing the waveform on test points 9 and 10 (TP9 and TP10).

The speech system clock appears on U3 pin 26. It should be 1.56MHz $\pm$ 1% for acceptance. The signal is termed RCL, or ROM CLOCK.

4.3 HARDWARE INITIALIZATION

4.3.1 The speech synthesizer U3 is reset via two lines: pin 2 and pin 25 (RESET and STANDBY-RESET, respectively). These are tied together and are tied to the *MSYNC line of the Master/Keyboard component. These signals are active low.

4.3.2 The buffer/interface chip, U2 is initialized by the game program code. For further information refer to the Mattel Electronics Component Specification #0086-0173.

4.4 MASTER COMPONENT -- CARTRIDGE -- U2 COMMUNICATION PATH

4.4.1 OVERVIEW

J1 is plugged into the Master Component and J3 connects to a game cartrdige. The microprocessor bus is fed to U2, with its associated bus control signals. The connector pinouts, though very similar in function, are not identical. Refer to Table 1 for an enumeration of these connector and chip pinouts and signal names.

TABLE 1

PIN #		FUNCTION		PIN #		FUNCTION	
U2	conn's *	J1	J3	U2	conn's *	J1	J3
19	1	GND	GND	12	23	DB12	DB12
25	2*	NC	C1		24	GND	GND
	3	*MSYNC	*MSYNC	13	25	DB13	DB13
26	4*	NC	C2		26	GND	GND
7	5	DB7	DB7	37	27	DB2	DB2
	6	EXTAUD	EXTAUD		28	GND	
8	7	DB8	DB8	14	29	DB14	DB14
	8	EXTVID	EXTVID	28	30*	NC	RCL
5	9	DB6	DB6	35	31	DB1	DB1
	10	MCLK	MCLK		32	BC1in	BC1in
9	11	DB9	DB9	33	33	DB0	DB0
	12	*RESET	*RESET		34	BC2in	BC2in
3	13	DB5	DB5	15	35	DB15	DB15
24	14*	NC	Sout(U3)		36	BDIRin	BDIRin
10	15	DB10	DB10	21	37	BDIR	BDIR
27	16*	NC	C3		38	BDIRout	BDIRout
1	17	DB4	DB4	22	39	BC2	BC2
16	18*	GND	Sin(U3)		40	BC2out	BC2out
11	19	DB11	DB11	23	41	BC1	BC1
	20*	GND	*REN		42	BC1out	BC1out
39	21	DB3	DB3	18	43	Vcc(+5V)	Vcc(+5v)
	22	GND	GND		44	GND	GND

* Indicates J1-J3 difference

4.4.2 MASTER COMPONENT -- CARTRDIGE COMMUNICATION PATH

Table 2 gives more information regarding the signals going between the master component and cartridge connectors, J1 and J3 respectively.

TABLE 2 DESCRIPTIONS OF SIGNALS BETWEEN J1 AND J3.

SIGNAL NAME	FUNCTION	POLARITY +/- *	CONNECTS TO: J3	CONNECTS TO: U2
BDIR out	Bus Direction out	+	38	
BC2 out	Bus cntrl signal 2 out	+	40	
BC1 out	Bus cntrl signal 1 out	+	42	
BC1 in	Bus cntrl signal 1 in	+	32	
BC2 in	Bus cntrl signal 2 in	+	34	
BDIR in	Bus Direction in	+	36	
*MSYNC	Master Resetting pulse	-	3	
BC1	Bus cntrl signal 1	+	41	23
BC2	Bus cntrl signal 2	+	39	22
BDIR	Bus Direction	+	37	21
VCC +5V	Power supply out to cart		43	18
DB15	Data/Address bus 15	+	35	15
DB14	Data/Address bus 14	+	29	14
DB13	Data/Address bus 13	+	25	13
DB12	Data/Address bus 12	+	23	12
DB11	Data/Address bus 11	+	19	11
DB10	Data/Address bus 10	+	15	10
DB09	Data/Address bus 09	+	11	9
DB08	Data/Address bus 08	+	7	8
DB07	Data/Address bus 07	+	5	7
DB06	Data/Address bus 06	+	9	5
DB05	Data/Address bus 05	+	13	3
DB04	Data/Address bus 04	+	17	1
DB03	Data/Address bus 03	+	21	39
DB02	Data/Address bus 02	+	27	37
DB01	Data/Address bus 01	+	31	35
DB00	Data/Address bus 00	+	33	33
MCLK	Mater Component Clock	+	10	
ExtAud	External Audio	Analog	6	
RESET	Reset input to M/C	-	12	
EXTVID	External Video Input	Analog	8	
GND	Ground		Several	19
CBLNK	CRT Blanking pulse	+	4	

* + indicates POSITIVE true logic
\- indicates NEGATIVE true logic

4.4.3 CARTRIDGE COMPATIBILITY

Non-Voice cartridges, when plugged into the cartridge slot on the 3330, produce shorts to ground on pins 16, 18 and 20 of J3. These signals are C3, Sin(U3), and *REN, respectively. In the Master Component, these conditions cause no problems, as these are either GND signals (18 and 20), or no connctions (16). Pin 16 is used in the Keyboard component and is handled by the circuitry associated with U1 and Q1. Pin 16 is not used by the cartridges. It is important to note that for qualification of the various chips, the signals C3, *REN, and Sin(U3) should be able to withstand indefinite shorts to GROUND. The Sin(U3) pin won't be damaged, as it is an input, but this signal line is connected to Sout of U2, and therfore could cause problems if the chip (U2) were not able to withstand such conditions.

4.4.4 MASTER COMPONENT - U2 INTERFACE BUS

The primary Master Component Microprocessor bus, 16 bits wide (DB0-15), with three control lines (BC1, -2, BDIR), are supplied to the buffer/interface chip. This bus carries information relevant to speech processor/peripheral-bus data/address transfers (i.e. those U2 responds to), and general game software signals (to which U2 does not respond actively). Note that the signals on J3-2, 4, 14, 16, 18, 20, and 30 are not sent to the Master Component. These signals are associated with the Voice Serial bus, and not with the Master Component microprocessor bus. They are enumerated in Table 1 for the purpose of completeness only, and are discussed in further detail in section 4.6

4.5 PARALLEL COMMUNICATION BETWEEN J2, U3 AND THE MASTER COMPONENT

4.5.1 OVERVIEW

The microprocessor in the Master Component uses U2 to commumicate with the speech synthesizer U3 and the stacking connector J2. The following groups of signals are involved: 2 U3 handshake lines, 8 bi-directional data lines, and 7 stacking connector control lines. The signals and their respective pin numbers are shown in Table 3.

TABLE 3 PARALLEL COMMUNICATION PIN-OUT

SIGNAL NAME AND GROUPING:	CONNECTS ON: U2	U3	J1	J2	J3	TP#
U3 Handshake lines						
*ALD	20*	20	---	---	---	TP5
*LRQ	17	9*	---	---	---	TP4
Bidirectional Data Bus Lines						
D0	32*	18	--	25	--	---
D1	34*	17	--	23	--	---
D2	36*	16	--	21	--	---
D3	38*	15	--	19	--	---
D4	40*	14	--	20	--	---
D5	2*	13	--	22	--	---
D6	4*	11	--	24	--	---
D7	6*	10	--	26	--	---
Stacking Connector Control Lines						
BC1	23	--	2	2*	41	---
BC2	22	--	1	1*	39	---
BDIR	21	--	6	30*	37	---
AD0	29*	--	8	--	--	---
AD1	30*	--	10	--	--	---
AD2	31*	--	9	--	--	---
RHMC	--	--	5	5	--	TP1

*..Indicates signal source.

4.5.2 . U3 HANDSHAKE LINES

4.5.2.1 OVERVIEW

These lines are used to coordinate the transfer of 8-bit parallel data from the Master Component to U3, through U2.

4.5.2.2 *LRQ (LOAD REQUEST)

When the speech processor is ready to accept parallel data, this line is brought low (U3 pin 9). It is received on pin 17 of U2, and is available on TP4.

4.5.2.3 *ALD

Upon receipt of a low signal level on *LRQ (U2-17), and when the Master Component performs a write to location 0080 (Hex), U2 passes the data to the 8-bit data bus lines. *ALD is strobed low, on U2-20. U3 receives this signal on pin 20. *ALD is available on TP5.

4.5.3 BI-DIRECTIONAL DATA BUS LINES

These 8 bi-directional lines originate on U2 (see Table 3). They are connected to the stacking connector (J2), and U3. Data appears on these lines whenever the Master component writes to certain addresses in the range 0080 to 0BFF (Hex). Refer to table 4, section 4.5.4.3.2 for details of this address range.

4.5.4 STACKING CONNECTOR CONTROL LINES

4.5.4.1 OVERVIEW

These 7 lines are used to control data transferrance from and to the stacking connector.

The signals can be grouped into two sections: those which represent Master component microprocessor bus control lines, and those generated by the 3330.

For information regarding the stacking connector jumper block (JB1, #3330-9609), this is contained in section .4.7.

4.5.4.2 MASTER COMPONENT BUS CONTROL SIGNALS

These signals, BC1, -2, and BDIR are fed to J2 as well as J3 and U2, from J1. They are generated by the microprocessor within the Master Component, and are used to coordinate address/data transferrance to the various system components. These components include any bus-controlled devices within J2-connected peripherals.

4.5.4.3 3330 GENERATED SINGALS

4.5.4.3.1 OVERVIEW

Three of these signals, (AD0, -1, -2) are used to address attached peripherals connected to the stacking connector, J2. The other, RMHC, controls bus-buffer direction in the Keyboard Component, allowing interface of the keyboard component to peripherals connected through J2.

4.5.4.3.2 AD0, AD1, AD2

These lines are used to provide 1-of-8 addressing codes for peripherals attached to J2. Table 4 gives the signal states for the various address ranges.

TABLE 4. ADDRESSES TRAPPED BY U2 AND RESULTING STATES OF AD0, AD1 and AD2

HEX ADDRESS	AD0	AD1	AD2
0080	0	0	1
0081	0	0	1
0082-00FF	0	0	1
01FE-01FF	1	0	1
0700-07FE	0	1	1
0800-08FF	0	0	0
0900-09FF	0	0	1
0A00-0AFF	0	1	0
0B00-0BFF	0	1	1
ANY OTHER	1	1	1

4.5.4.3.3 RHMC (REMOTE HAND CONTROLLER)

This signal originates at the collector of Q1 (PN2906, #0086-0330). This line acts on the Keyboard component bus buffers, to reverse their direction. This signal is normally LOW. It is derived from AD0, AD2, BC1, and BDIR, and must be able to pull a grounded 1Kohm ±5% resistor up to a level of 4.5V ± 10%.

TP2 is the output of U1A, whose inputs are HIGH, HIGH, and BDIR.

TP3 is the output of U1B, whose inputs are HIGH, AD0, and AD2.

TP1 is the output of the logic network.

Resistors R2, R4 and R5 are pull-up resistors for the open-collector outputs of U1. They are to be 2.2K Ohm 5% resistors (#0095-0861).

Resistor R3, 180 Ohm (#0095-0601), limits the collector current of Q1.

Resistor R1, 1.0K Ohm (0095-0781), limits the base current of Q1.

Each pulse from the network, when driven by a standard and correct Master component, should be 2 ± 10% us long, with rise time of 35 ± 10% ns.

Fall time is to be measured with the circuit connected to a 1 Kohm resistor to Ground. The fall time of the circuit should be less than 0.5 ± 5% us.

4.6 SERIAL SPEECH DATA PATH

4.6.1 Overview

Data is serially transferred on the serial bus between U2 and U3 via the Sin and Sout pins of both chips. The bus is controlled by the C1, C2, C3 signals, and is synchronous with RCL. *REN is sent to J3, but not to the buffer/interface chip U2. Data can also be serially transferred in and out of the game cartridge via the serial bus brought to the cartridge connector. The signal names that pertain to the serial bus are shown in Table 5, with their respective pin assignments.

TABLE 5 VOICE SERIAL BUS PIN ASSIGNMENTS

Chip/Signal: / Connector:	Sin	Sout	*REN	C1	C2	C3	RCL
U2	24	16	----	25	26	27	28
U3	21	12	3*	4*	5*	6*	26*
Cart.; J3	18	14	20	2	4	16	30

*..Indicates signal source. Sin is an Input, Sout is a Tri-state output for all devices (U2 and U3).

As shown, Sout of U3 is tied to Sin of U2, and vice versa. The connector J3 has designations coordinated with the signals of U3.

4.6.2 Sin AND Sout

Data is serially produced on the Sout pins of U2, U3, and J3-14 (to be connected to a game cartridge with suitable voice serial ROM). These must be tri-stateable outputs.

Data for U2, U3, and J3-18 is received on their respective Sin pins. These are standard MOS inputs.

4.6.3 *REN (ROM-ENABLE)

Pin 20 of the 3330's cartridge connector (J3) is connected to the ROM-ENABLE (pin 3) output of U3.

Note that with some game cartridges (pre-voice and non-voice), pin 20 is grounded.

4.6.4 RCL (ROM-CLOCK)

The ROM clock, RCL, is a derivative of the clock input, and should be within 1% of the nominal frequency, 1.56 MHz.

The RCL signal should be active whenever the RESET pins (cf. section .4.3.1) are high.

4.6.5 C1, C2, AND C3

These signals (see Table 5 for appropriate signal locations), are used to control the Voice serial bus. Their various states are used to indicate the function and destination of the data on the serial bus, or as a strobe signal for certain built-in functions of the chips (U2, U3 and cartridge serial voice ROM, if present). See the individual specifications for more detailed descriptions of the functions.

4.7 STACKING CONNECTOR JUMPER BLOCK

4.7.1 OVERVIEW

J2, when not connected to any other peripherals, requires a jumper-block ,(JB1, #3330-9609), to be in place to allow the 3330 unit to function. The jumper block shorts pins 3 & 4, and 27 & 28.

The unit, nor the game cartridge will be supplied power without this part, or its electrical equivelent.

4.7.2 POWER SUPPLY BOOSTING/SUPPORT

The connector, J2, has its connections arranged in such a way as to allow a future power supply to fill the 3330 and game cartridge power requirements, and boost the power capability of the Master/Keyboard component's power supply.

Power received from J1 pin 43 is sent to J2 pin 4. Without any peripherals attached to J2, there should be a shorting block to short pins 4 and 3. The input voltage is available for test on TP7.

Master/Keyboard component power supply boosting can be accomplished by allowing power input to the 3330 stacking connector, J2-6. Through R26, 8.2 Ohm, 2W 5% (0084-0927). This unregulated voltage (Vunreg, J2-6) is applied to the Master/Keyboard component Vcc, on J1 pin 43 to supply approximately 270mA boost.

4.7.3 MCLK SIGNAL LOOP ROUTING

Also provided for with the stacking connector is the ability of future products located on the stacking connector to access and use MCLK, a Master Component supplied clock signal. This signal is received on Pin 10 of J1, sent to J2-27, again received on J2-28, and finally sent out to the Cartridge connector J3. The 3330 does not actively use or change this signal in any way, but the signal path is required for compatibility with past and future products.

4.8 AUDIO OUTPUT

4.8.1 OVERVIEW

The audio output of the 3330 Voice Synthesis module consists of a multi-stage filter/amplifier section. Supplying these is a voltage reference section. These all combine to change the pulse width modulated output of U3 to an analog signal suitable for combining with the Master Component sound signal.

4.8.2 FILTER RESPONSE

Referring to Figure 3, a composite spectrum graph of the nominal, high and low tolerance limits of the analog filter/amplifier. This filter has the characteristics of a five-pole Low pass elliptic filter, a two-pole High pass filter, and a uni-polar Low pass filter in combination. These measurements were taken with U2 in the RESET mode, and with the Logrithmic reference level (0dB) being taken as the output level of the circuit at 400Hz $\pm$ 10%. The Volume control shall be set to its maximum counter-clockwise position (full-on).

The high-pass pole charateristics are that of two poles that are isolated from each other. The higher pole for this element is to be 400 Hz $\pm$ 10%. The lower pole is set at approximately 100 Hz $\pm$ 10%, and causes a -6dB/Octave rolloff below approximately 200Hz ($\pm$10%).

The uni-pole Low pass operates within the overall range of the bandpass (150Hz -5KHz), and provides Bass pre-emphasis at the rate of approximately -3dB/Octave.

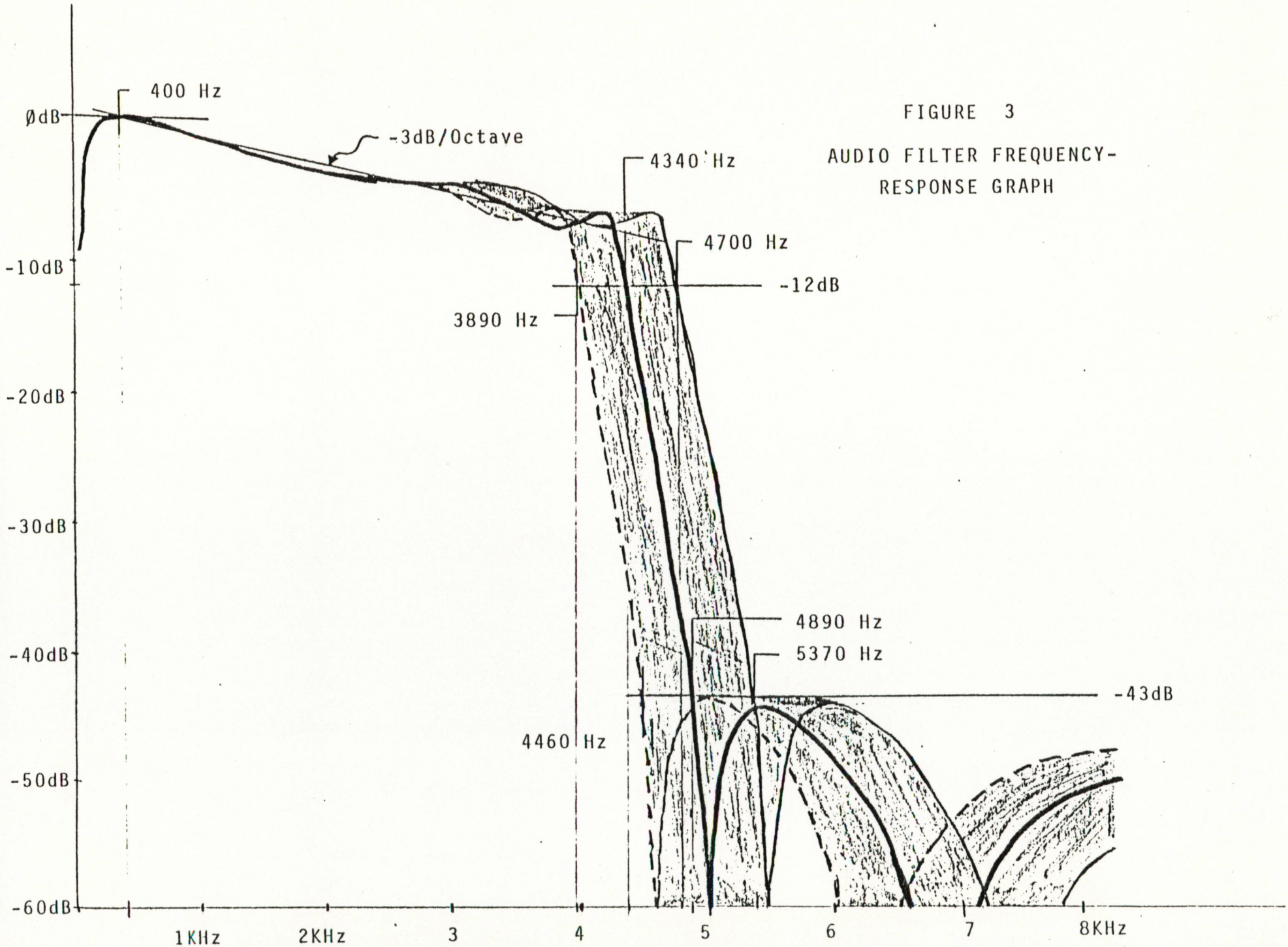


FIGURE 3

AUDIO FILTER FREQUENCY-RESPONSE GRAPH

The five-pole elliptic filter's cutoff characteristics are that shown within and to the right of the knee of the graph. It has a slope of approximately -120 dB/Octave (±10%), and drops from a level of -12dB (at 4340Hz, ± 10%), to -44dB at 4890Hz ± 10%. This level (-44dB) represents a level above which the response of the circuit should not extend for any frequency above 5KHz. The first major null occurs at 5KHz ±5%. The second major null in this section occurs at 6.5KHz ±10%.

4.8.3 GENERAL OPERATION

Input to the filter is from the open collector output of U3 pin 24. R9 and R10 (330 Ohm, 5% each, #0095-0661) are the open-collector load. Input to the filter is taken from the junction of R9 and R10. This reduces the input swing to one-half the supply voltage, thus preventing saturation of the Op-Amps, U4 (LM324C, #0098-1210) and U5 (LM358C, #0086-0170).

Bias current to the non-inverting input of U4C and U4A is provided through R15 and R20 (8.2K Ohm 2%, #0084-0092 each) from 1.8V. Bias for U4B and U4D is provided through R22 (200K potentiometer, #3330-0030), R21 (12K 5%, #0095-0996), R17 (12K Ohm, 2%, #0084-0377), R16 (16K Ohm 2%, #0084-0405), and R12 (3.9K Ohm 2%, #0084-0345).

Gain control is provided by R22 which feeds amplifier U5A, R23 (12K Ohm 5%, #0095-0996), and R24 (22K Ohm 5%, #0095-0182). This amplifier should have a maximum gain of 4.9 ± 5%. R22 has a value of 200K Ohm, ± 20%.

R22 also works with C8 (0.0047uF 5%, #0085-2630) to provide one of the High-pass filter poles. The value of R22 was selected such that the cutoff frequency of the high pass-pole is provided by C9 (4.7uF 10V Minimum, #0085-0025) and R25 (430 Ohm, ± 5%, #0085-0691).

In the passband of the filter (150Hz to 5Khz ±10%), signal flow is through C3 (0.0047uF 5%, #0085-2630), R11 (16K 2%, #0084-0405), R16, R21, R22, U5A, C9, and R25.

Outside of the passband (at low frequencies), the same applies, with C3 and C9 impeding the signal.

At high frequencies (above 5KHz), the signal is shunted through R12 and R17 and the op-amp networks. When the impedance of the op-amp networks equal its series resistor, an effective short circuit to the artificial Ground (+1.8V with respect to the logic Ground) appears at either end of R16. This action greatly reduces the output signal amplitude as indicated in the frequency response plot, Figure 3.

4.8.4 FILTER DERIVATION AND THEORY

4.8.4.1 INTRODUCTION

This explanation, due to the complexity of the filter, contains some terms which may not be familiar to those not heavily versed in Electronic Theory.

Space limitations force the omitting of descriptions for many of these terms. Thus, this section is intended for reference only by those already familiar with the concepts contained herein.

4.8.4.2 DERIVATIONAL OVERVIEW

The low pass section was developed from standard filter configuration tables. Using impedance transformation, all parameters were multiplied by 1/s. Then, using a GIC element (Generalized Impedance Converter) to create the desired FDNR element (Frequency Dependent Negative Resistor).

Figure 4 shows the theoretical low pass filter, before the conversion.

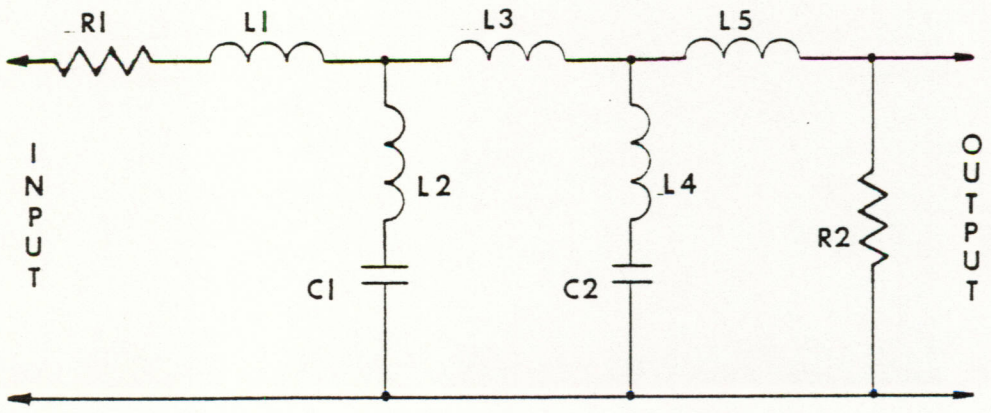


Figure 4

R1 and R2 are input and output terminating resistors, respectively. L1 and C1 provide 2 poles of low pass filtering. L3 and C2 provide 2 more poles. L5 and R2 provide the 5th pole. At a frequency determined by L2 and C1, series resonance occurs, which provides a null. Similarly, a null is also produced by L4 and C2. These frequencies can be calculated by the following equation.

$$f = \frac{1}{2\pi C \sqrt{R \cdot R4}}$$

Where R is either (from the schematic) R12 or R17 and R4 is either R14 or R19 and C is either C4·C5 or C6·C7.

The first notch in the filter response appears at 6810Hz, and the second at 4995Hz.

The above equation assumes that R13 = R15 and R18 = R20 (from the schematic).

The total filter response is as shown in Figure 3, and described in section 4.8.2.

If all elements of the filter in Figure 4 are multiplied by the same factor, the filter characteristics remain unchanged. When the multiplying factor is 1/s, then the nature of the elements change. Refer to Figure 5. Inductors become resistors, resistors become capacitors, capacitors become FDNR's, shown as 'D' elements.

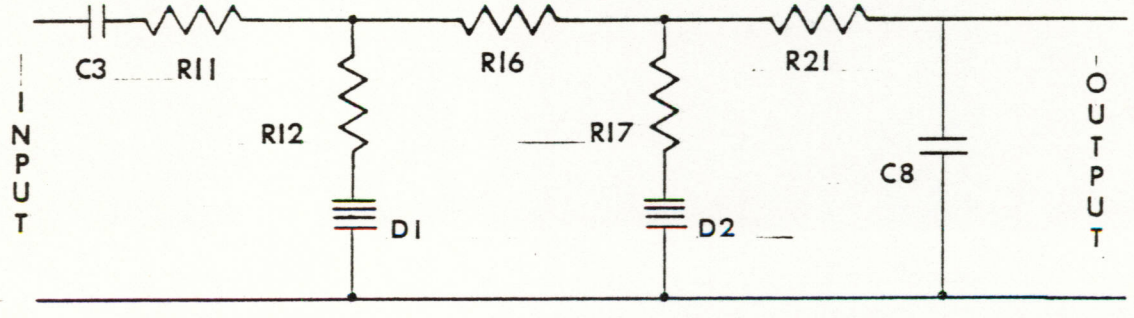


Figure 5.

Figure 5 uses the same reference symbols as are shown on the schematic Rev H. D1 and D2 and FDNR's, which can be produced by using the GIC element shown in Figure 6.

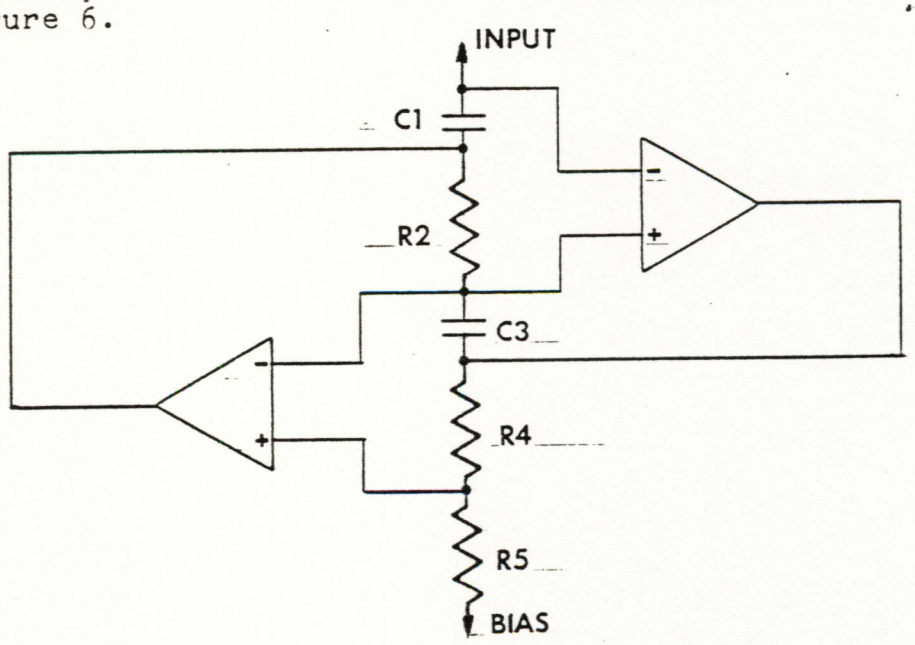


Figure 6

$$D = \frac{C1 \cdot C3 . R2 \cdot R4}{R5}$$

If C1 = C3 and R2 = R5

$$D = C^2 \cdot R4$$

The impedance of this element is:

$$Z = -\frac{1}{(2\pi f)^2 \cdot D}$$

Thus, the desired Frequency Dependent Negative Resistor is obtained.

Referring to the schematic and Figure 7, C corresponds to C4 and C6. R2 corresponds to R13 and R18; C3 to C5 and C7; R4 to R14 and R19; R5 to R15 and R20.

4.8.4.3 FILTER OUTPUT AMPLIFIER

At the ouptut of the low-pass filter is the volume control R22, and the amplifier U5. The output of U5 is fed through the uni-polar low pass filter with the slope described in section 4.8.2 . The components making up this section of the circuit include R24, C14, and R23 (22Kohm ¼ Watt 5%; #0095-0102, 4700pF 5% 10Vmin; #0085-2630, and 5.6Kohm ¼ Watt 5%, #0095-0961 respectively)

Also at the output of the amplifier U5 is a filter component which gives the High pass poles of the filter (i.e. the pole at 150Hz and 400Hz). This section is composed of C9 and R25 (4.7uF 10V -10%,+50%, #0085-0025, and 430 ohm ¼ Watt 5% #0095-0961, respectively).

4.8.4.4 FILTER/AMPLIFIER BIAS GENERATOR

One-half of U5 is used to create a bias potential for use by the filter and amplifier. It is formed from a resistive divider network of a 180 K ohm ¼ Watt 5% (R7, 0095-0322) resistor, and a 100K ohm ¼ Watt, 5% (R8, 0095-0262) resistor. The amplifier is used in closed-loop unity gain configuration (U5-7 & 6 shorted). The bias voltage appears on U5-7, and should be 1.80 V ± 10%. C2 (10uF 16V +10%,-50%, 0085-0003) and C13 (0.01uF, 10V, ceramic disc, 0096-4020) were added to increase the stability and drive capabilities of the bias generator.

4.9 POWER SUPPLY CONSIDERATIONS

Power consumption for the 3330 averages 150 mA @ 5VDC.

The current draw should be less than 200 mA, and more than 130 mA to be considered normal. Refer to Table 6 for a listing of the Voltage and current margins/limits.

At present, the power for the 3330 is supplied by the Master/Keyboard component.

TABLE 6 POWER SUPPLY MARGINS

VOLTAGES, V_{cc} to GROUND

I Limits @:	4.5V	5.0V	5.5V
High	160 mA	170 mA	180 mA
Low	110 mA	120 mA	130 mA

4.10 TEST POINTS AND EXPECTED SIGNAL FORMS

Figure 7 shows the solder side of the PC board, and gives information about the various circuit test points. The information provided on the figure includes: Equipment calibration information, signal names, test point numbers, and any other helpful data. All reference designations are taken from the schematic, # 3330-9259.

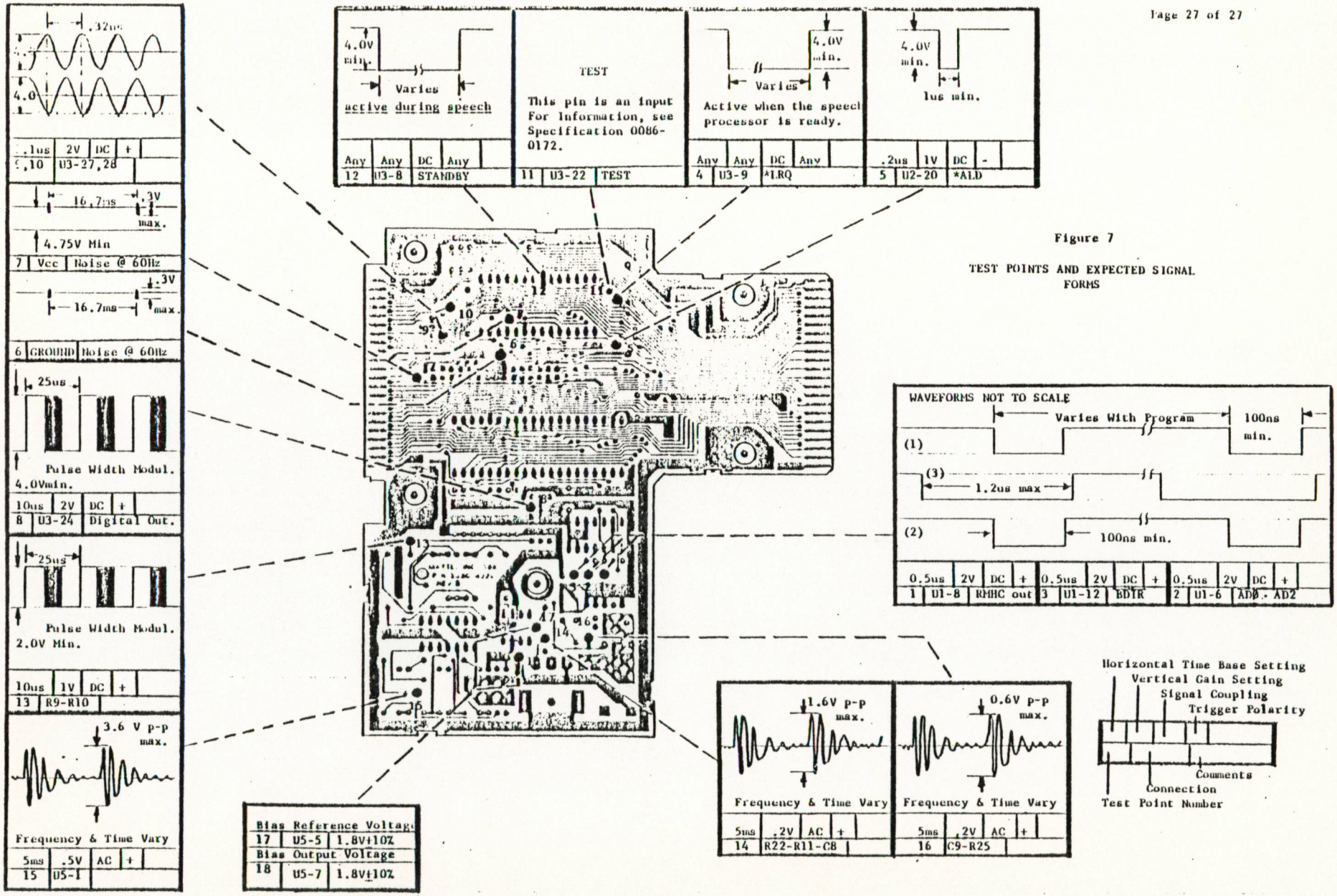


Figure 7

TEST POINTS AND EXPECTED SIGNAL FORMS

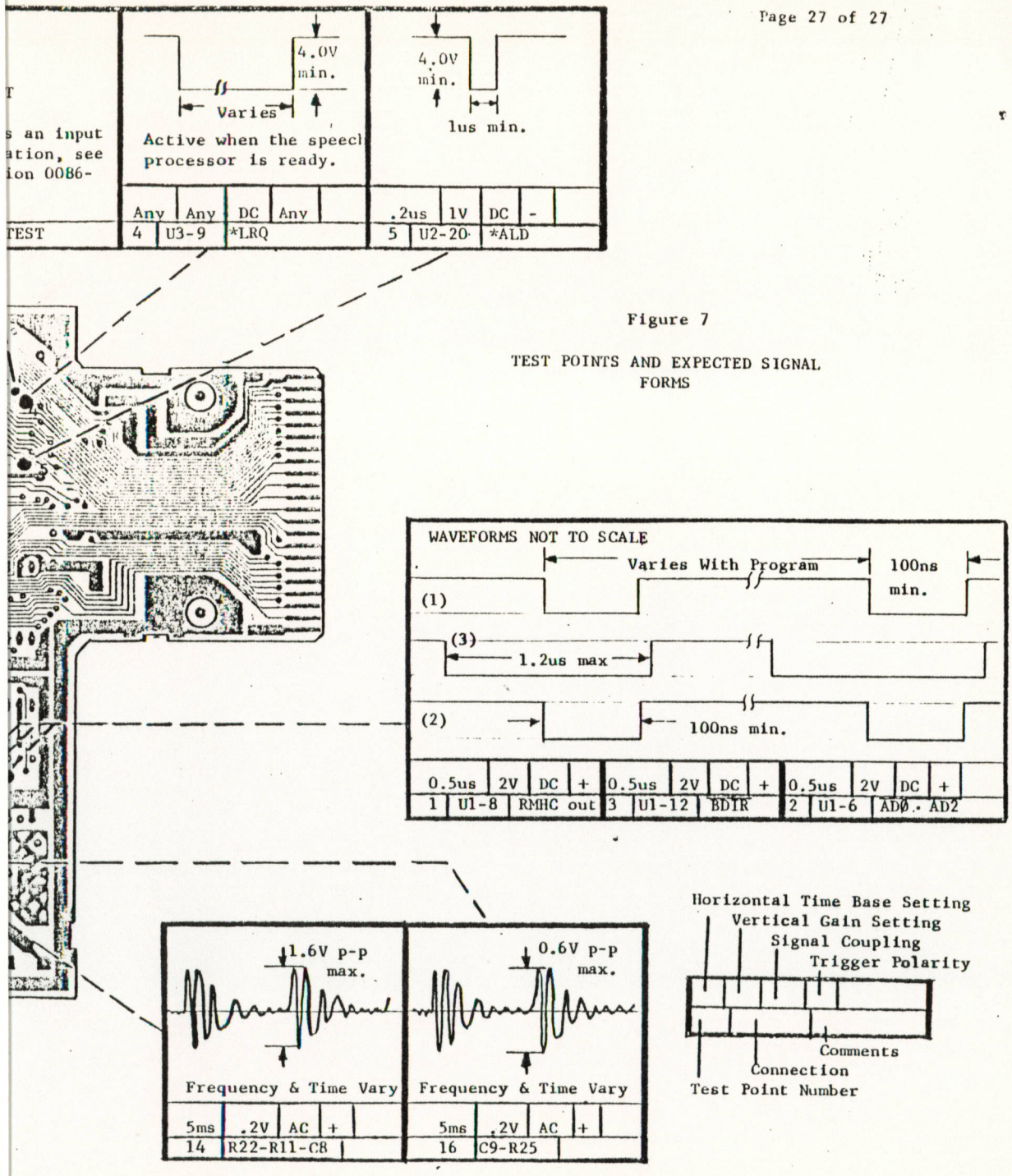


Figure 7

TEST POINTS AND EXPECTED SIGNAL FORMS

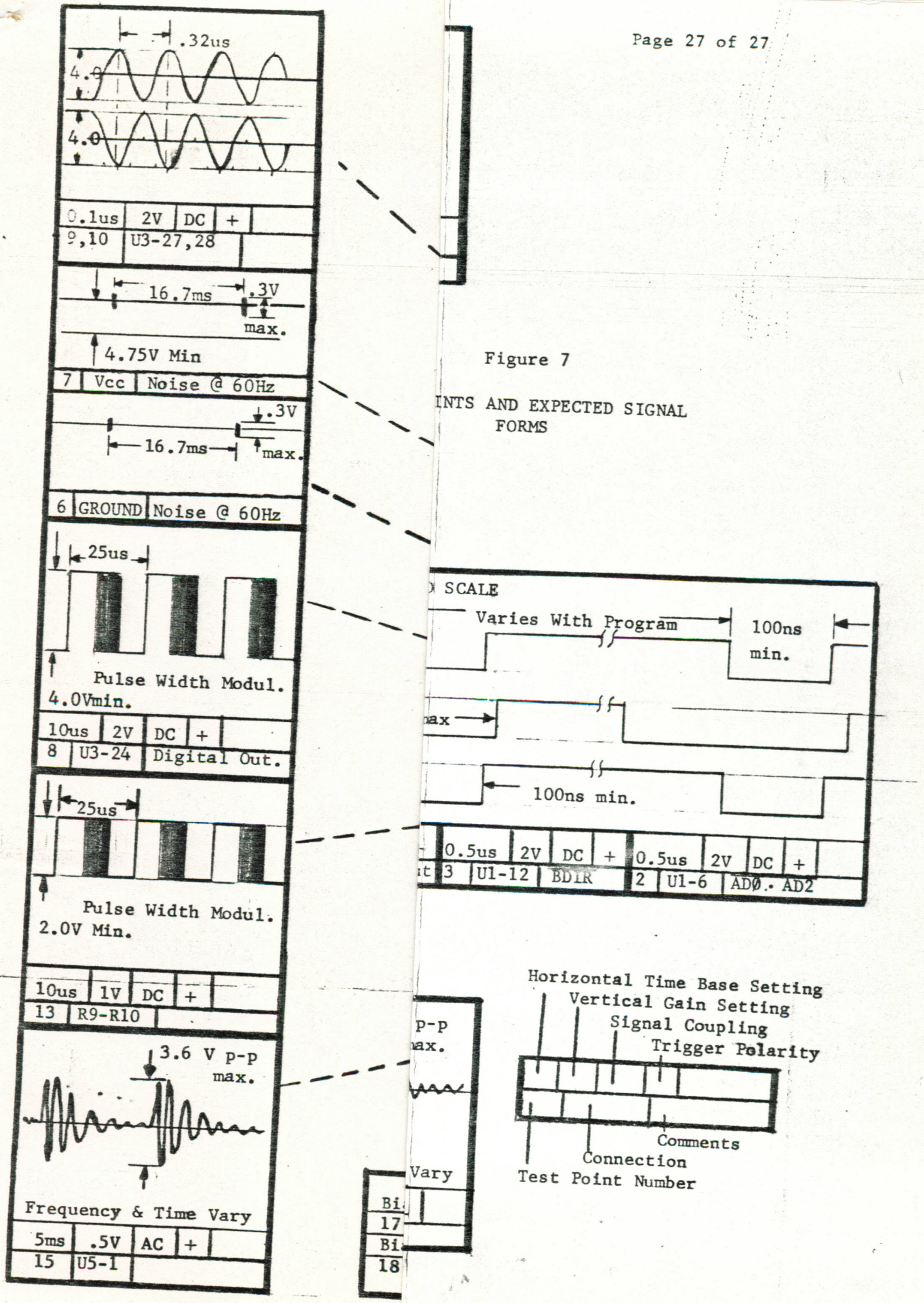


Figure 7

INTS AND EXPECTED SIGNAL FORMS

REVISIONS MAT—3213

PAGE 1 OF

EFFECTIVITY	AUTH.	LTR.	DESCRIPTION	DATE	APPROVED
		N/A	Initial Release	JUL 30 1982	

REV.																											
SHEET																											
REV. STATUS OF SHEETS	REV.																										
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

CONTRACT NO.

WRITTEN [signature] 6/15/82

CHECKED

ENGR. — — —

PROJ. ENGR. J. Randolph 7/28/82

Q.A. J. RIVANI 7/19/82

OTHER

MATTEL ELECTRONICS

MATTEL ELECTRONICS, a division of MATTEL, INC.

5150 ROSECRANS AVENUE, HAWTHORNE, CALIFORNIA 90250

Specification - Speech Buffer, I.C., interface for Voice Synthesizer

0086-0173

1.0 SCOPE

The specification establishes the requirement for a custom interface circuit for 640-bit Speech Buffer to a Voice Synthesizer.

2.0 APPLICABLE DOCUMENT

General Instrument

CP1600 Data Manual

DOS SP-0256 - Design Objective Specification for the Speech Processor.

DOS SPR-016, SPR-032, SPR-128 - Design Objective Specification for the Speech ROMS - 16K, 32K, or 128K

3.0 PURPOSE

The Speech Buffer shall be a 10 bit X 64 word FIFO (First-In, First Out) buffer memory capable of interfacing between the General Instrument CP1600/CP1610 series of micro processors, and the SP-0256 Speech Processor. This device will extend the range of applications of the SP-0256 to micro processor based systems.

The Speech Buffer shall be capable of interfacing to the Mattel Electronics STIC system, via the cartridge port, so that the speech system can be added to the master component. Auxiliary address mapping on the Speech Buffer shall increase the amount of addressable memory available to the master component, making the Speech Buffer the interface device for other than speech significant system upgrades.

4.0 REQUIREMENTS

4.1 The D.C. characteristics shall be as presented in Table 1.

4.2 The A.C. characteristics shall be as presented in Table 2 and Figures 8-12.

4.3 Electrical characteristics shall be as presented in Table 3.

4.4 Process and Die Size

The die size in standard N-Channel Metal Gate technology will be between 180 and 135 mils on a side in sub-alpha (90-32000) design rules.

4.5 SPB Addresses

The Speech Buffer addresses shall be as shown in Table 4 and the Speech Buffer shall be as shown by the block diagram in Figure 1.

4.7 Control States-Functions

The Speech buffer C1, C2 and C3 control states shall be as shown in Table 5.

4.8 Write/Read Characteristics

Write/Read modes shall be as shown in Figure 2 thru Figure 7.

4.9 Timing Diagrams

Timing diagrams shall be as shown in Figure 8 thru 11.

4.10 Address Select/Deselect

Address select and address deselect shall be as shown in Figure 12.

4.11 Speech Buffer Pinout

The Speech Buffer pinout shall be as shown in Figure 13.

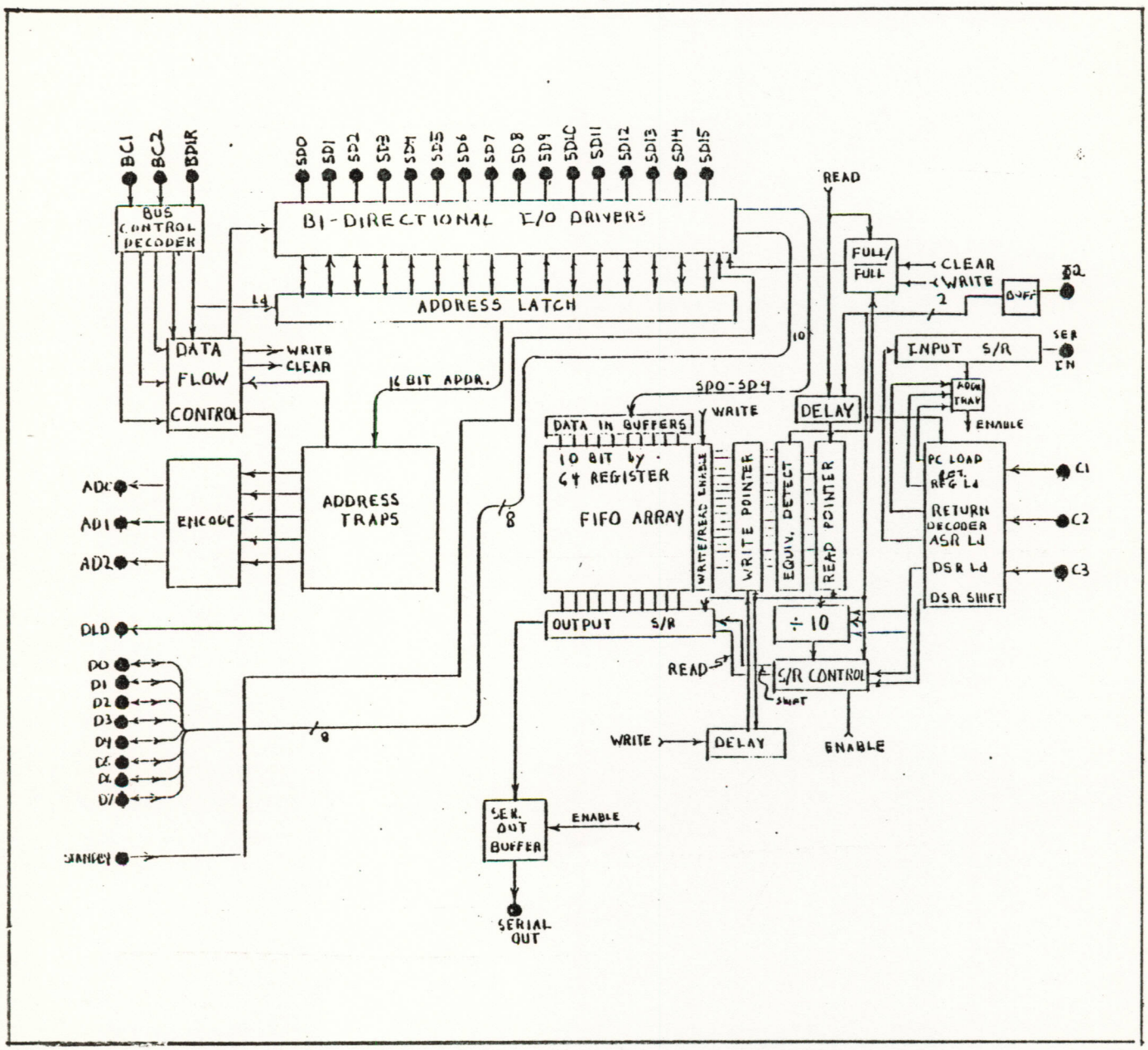
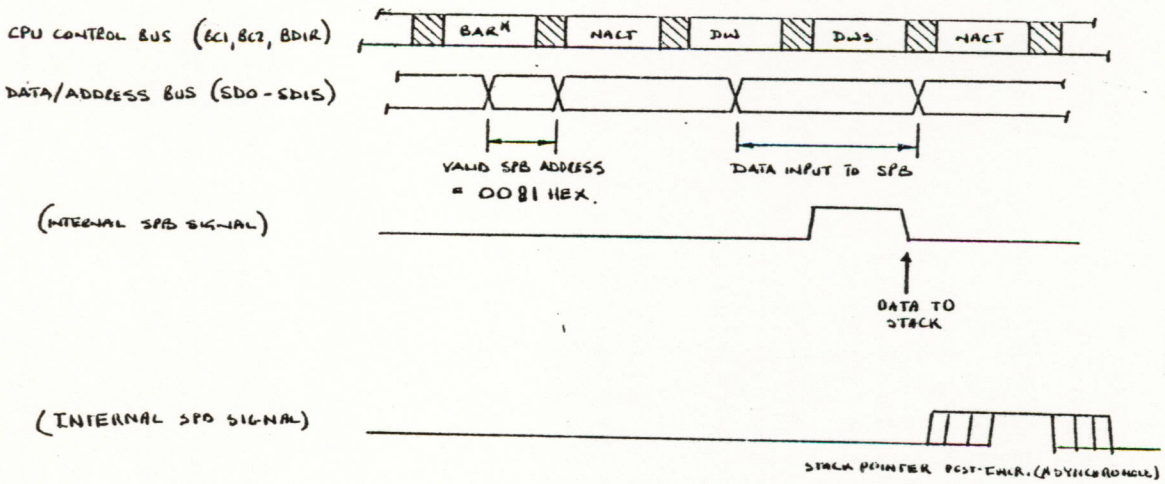

BC1
BC2
BDIR
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
BUS CONTROL DECODER
BI-DIRECTIONAL I/O DRIVERS
READ
FULL/ FULL
CLEAR
WRITE
BUFF
BZ
ADDRESS LATCH
LA
DATA FLOW CONTROL
WRITE
CLEAR
16 BIT ADDR.
10
INPUT S/R
SER IN
SD0-SD9
DATA IN BUFFERS
WRITE
DELAY
ADDR TRAV
ENABLE
10 BIT by 64 REGISTER FIFO ARRAY
WRITE/READ ENABLE
WRITE POINTER
EQUIV. DETECT
READ POINTER
PC LOAD REG LA
RETURN DECODER ASR LA
DSR LA
DSR SHIFT
C1
C2
C3
AD0
AD1
AD2
ENCODE
ADDRESS TRAPS
8
DLD
D0
D1
D2
D3
D4
D5
D6
D7
8
OUTPUT S/R
÷ 10
READ
S/R CONTROL
SHIFT
WRITE
DELAY
ENABLE
STANDBY
SER. OUT BUFFER
ENABLE
SERIAL OUT

Figure 1

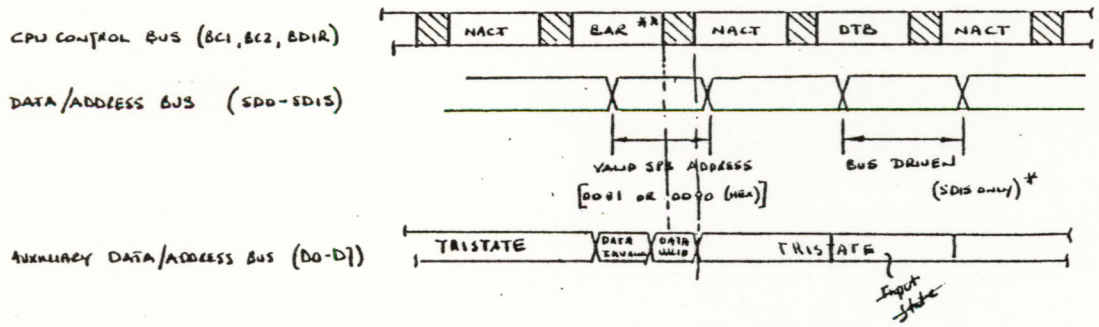
Figure 2



CPU WRITE TO STACK.

*NOTE: BAR COULD ALSO BE ADAR OR INTAK

Figure 3

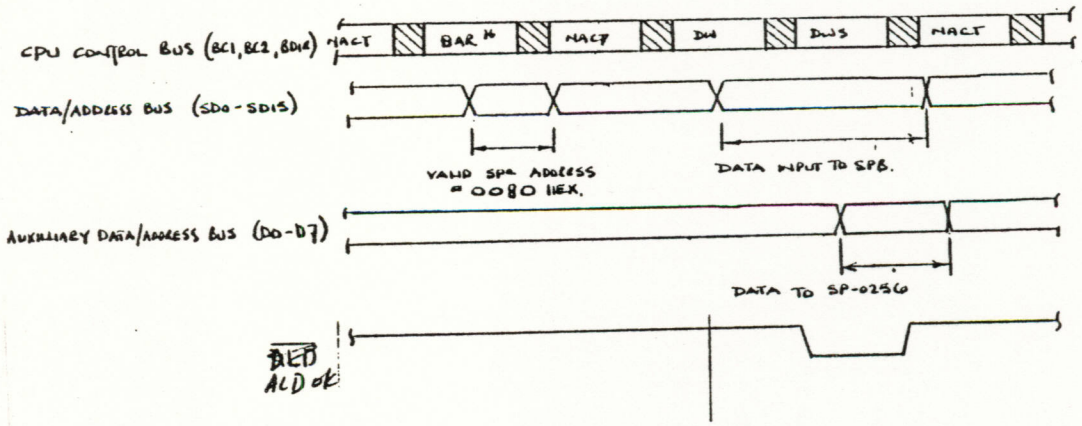


*NOTE: ONLY SDIS CONTAINS DATA – ALL OTHERS ARE AT LOGICAL "0"

** BAR COULD ALSO BE ADAR OR INTAK

CPU READ SPB – STATUS TO CPU BUS

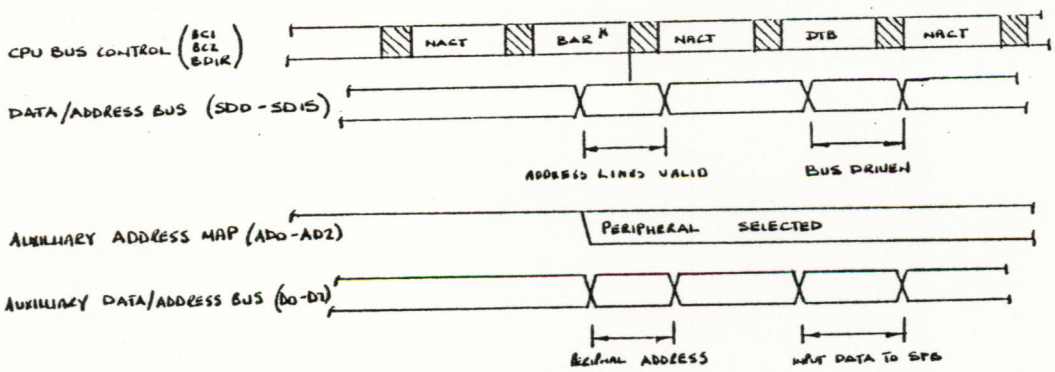
Figure 4



CPU WRITE TO SPEECH PROCESSOR

*NOTE: BAR COMD ALSO BE AD AR OR INTAK

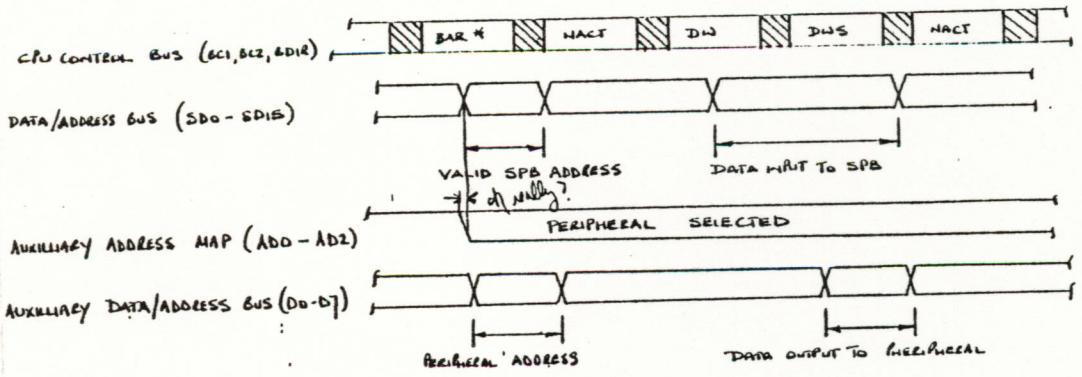
Figure 5



CPU READ CYCLE BUS COPY [D0-D7] TO [SD0 - SD15]

*NOTE: BAR COULD ALSO BE ADAR OR INTAK

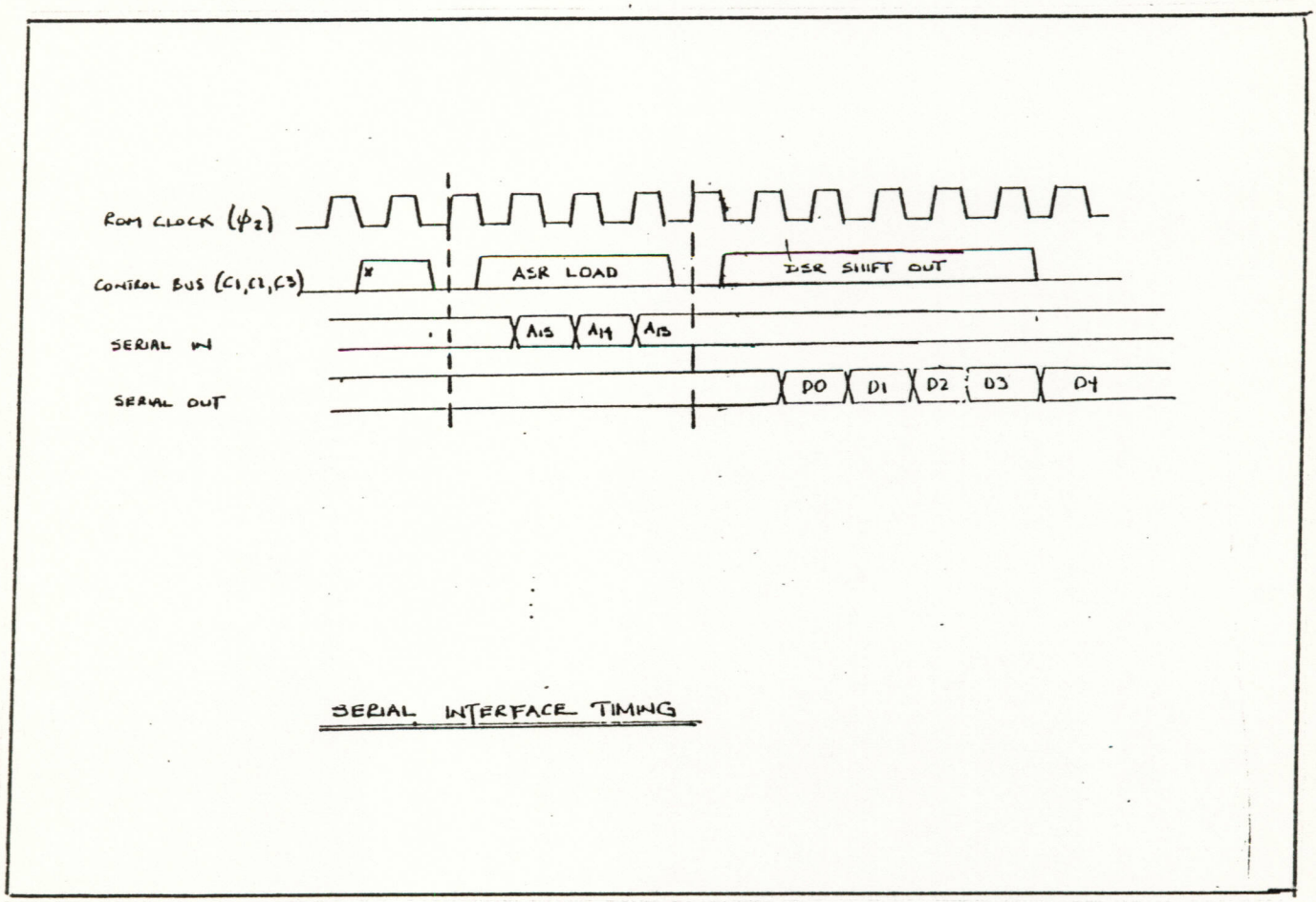
Figure 6



CPU WRITE CYCLE BUS COPY [SD0-SD15] TO [D0-D7]

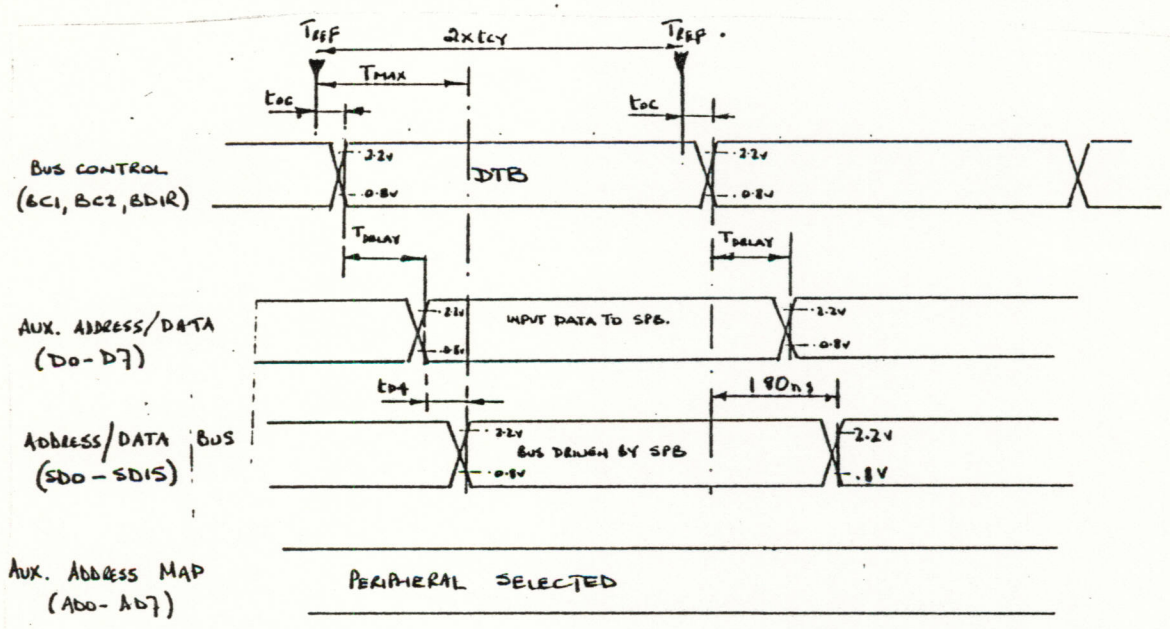
*NOTE: BAR COULD ALSO BE ADAR OR INTAK

Figure 7



SERIAL INTERFACE TIMING

Figure 8



NOTES:- (i) tcy = CYCLE TIME ± 50nS @

(ii) FROM CPU000 DATA

t_{DC} = 100nS max

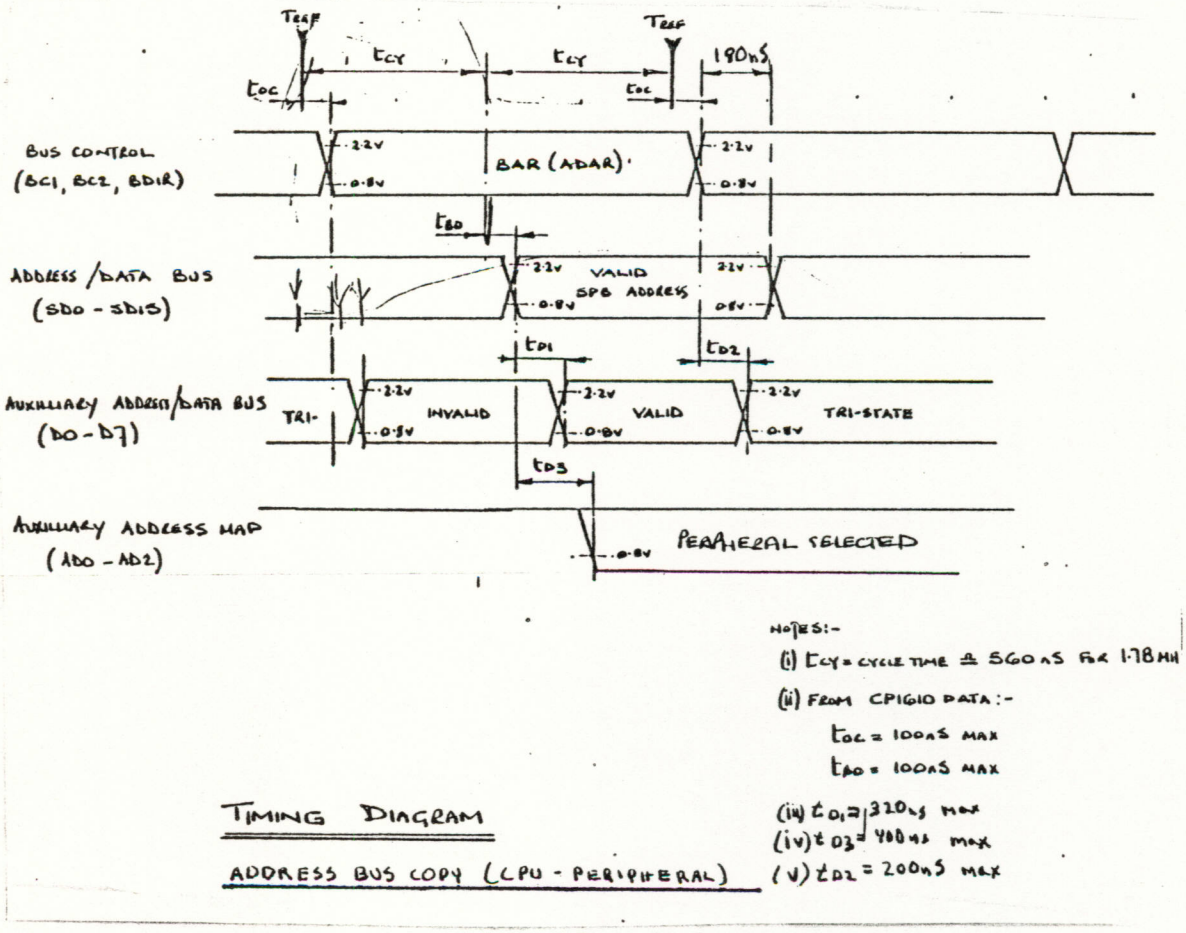
(iii) T_{DELAY} = external logic delay

(iv) T_{MAX} = 550nS.

(v) t_{DF} = 240 ns max

TIMING DIAGRAM - DATA BUS COPY (PERIPHERAL- CPU).

Figure 9



NOTES:-

(i) t_{CY} = CYCLE TIME ≥ 560nS FOR 1·78MH

(ii) FROM CP1610 DATA:-

t_{DC} = 100nS MAX

t_{BD} = 100nS MAX

(iii) t_{D1} = 320nS MAX

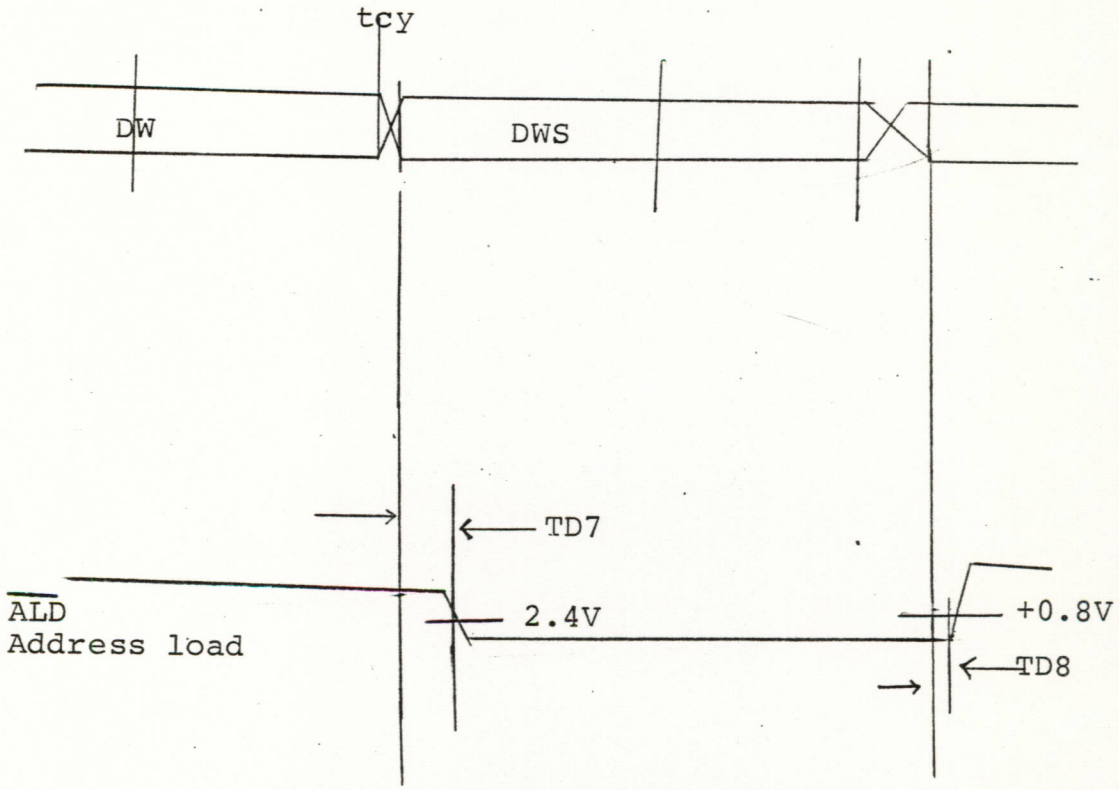
(iv) t_{D3} = 400nS MAX

(v) t_{D2} = 200nS MAX

TIMING DIAGRAM

ADDRESS BUS COPY (CPU - PERIPHERAL)

Figure 10



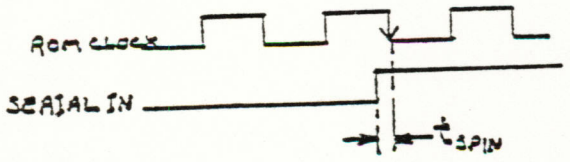
Note: TD7 = 180us
TD8 = 200us max

Figure 11

SERIAL AC CHARACTERISTICS

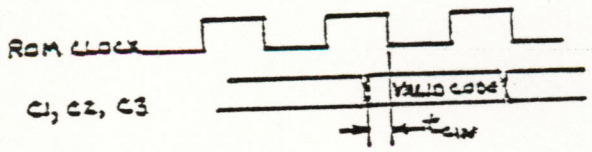
1. SERIAL-IN Set-Up Time

(t_{SPIN}) is the time that the SERIAL INPUT has to be valid before the falling edge of ROM CLOCK for correct functionality.



2. CONTROL BUS Set-Up Time

(t_{CIN}) is the time that the control bus inputs, C1, C2 and C3, have to be valid before the falling edge of ROM CLOCK for correct functionality.



3. SERIAL OUTPUT ACCESS TIME

(t_{ACC}) is the delay time from the falling edge of ROM CLOCK that is coincident with the control bus code = DSR SHIFT or DSR LOAD, to the data becoming valid on the SERIAL OUTPUT

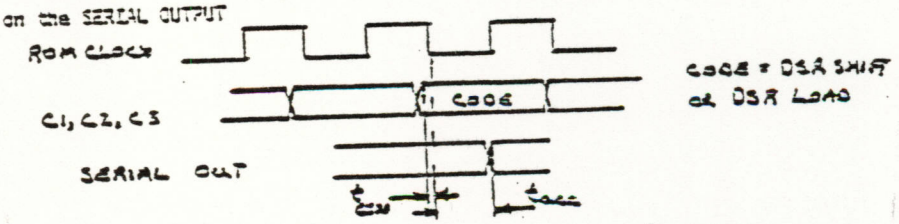
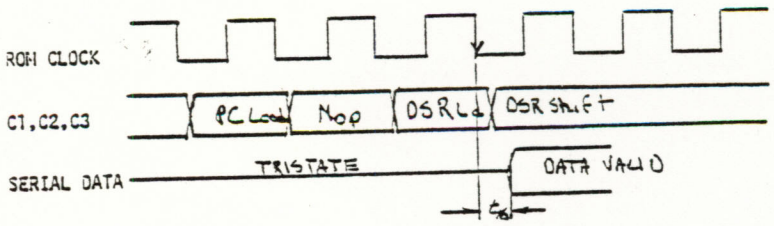


Figure 12

4. ADDRESS SELECT ACCESS TIME

(t_{AS}) is the delay time from the falling edge of ROM CLOCK that is coincident with a DSR Ld instruction to the serial data bus outputting valid data. This occurs after a valid address has been loaded into the "PC".



5. ADDRESS DE-SELECT ACCESS TIME

(t_{AD}) is the delay time from the falling edge of ROM CLOCK that is coincident with DSR Load instruction to the serial data bus going into tristate. This occurs after an invalid address has been loaded into the "PC".

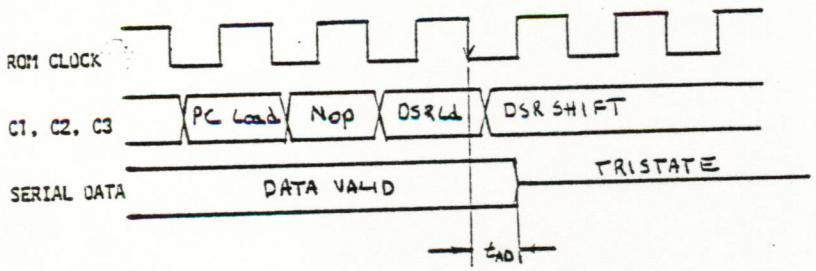
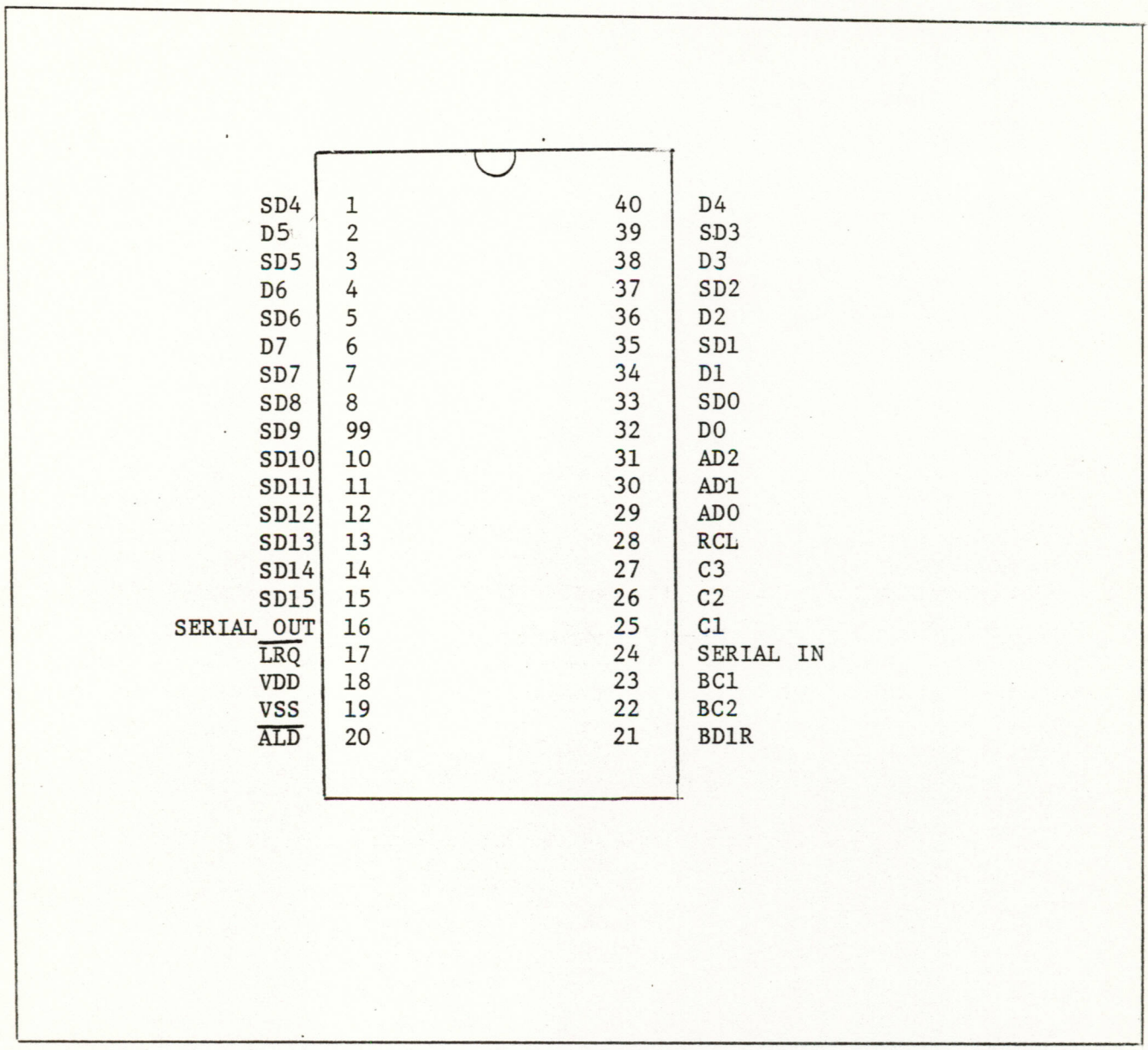


Figure 13


SD4 1
D5 2
SD5 3
D6 4
SD6 5
D7 6
SD7 7
SD8 8
SD9 99
SD10 10
SD11 11
SD12 12
SD13 13
SD14 14
SD15 15
SERIAL OUT 16
LRQ 17
VDD 18
VSS 19
ALD 20
40 D4
39 SD3
38 D3
37 SD2
36 D2
35 SD1
34 D1
33 SD0
32 D0
31 AD2
30 AD1
29 AD0
28 RCL
27 C3
26 C2
25 C1
24 SERIAL IN
23 BC1
22 BC2
21 BD1R

"POWER UP" CONDITIONS"

1. Upon applying power to the Speech Buffer the following conditions will exist:

   a. The parallel (CP1600) Address Register will hold a "random" address In addition the RAM's read and write pointers will be in an invalid state.

   b. The "PC" may or may not hold a valid SPB address.

   c. The serial out pin may or may not be in Tristate.

2. To place the Speech Buffer in a known state the following steps must be taken:

   a. Execute a "clear" instruction (See table 1, page 12). This will alleviate condition "1a" above.

   b. Shift in an address on the serial in pin and execute a PC Load.

   c. Execute a DSR load. The serial out pin will now be on the bus if and only if the valid Speech Buffer Address was shifted in as explained in "2b" above.

TABLE 1

MEASUREMENT	SYMBOL	MIN	MAX	UNITS	CONDITIONS
Power	V_{DD}	4.65	6.0	V	
	I_{DD}		82	mA	@ T_{AMB} = 25°C
Temperature	T_{AMB}	0	70	°C	
Leakage	I_L		10	uA	Input foreced to 7.5V
(tristate)	$I_{L(TS)}$	-10	+10	uA	In put forced to 0V or V_{DD}.
Output Drive DØ-7	V_{OL}		0.4	V	I_{OL} = 2.5mA
	V_{OH}	2.4		V	I_{OH} = -200uA
Output Drive ADØ-2	V_{OL}		0.6	V	I_{OL} = 1.8mA
	V_{OH}	2.4		V	I_{OH} = -125uA
Output Drive SDØ-15, $\overline{ALD}$, S_{OUT}	V_{OL}		0.6	V	I_{OL} = 1.0mA
	V_{OH}	2.4		V	I_{OH} = -125uA
Input levels C1, C2, C3	V_{IL}	0	0.65	V	
	V_{IH}	2.35		V	
Input Levels	V_{IL}		0.7	V	
	V_{IH}	2.35		V	

Note: All measurements at T_{AMB} Maximum unless otherwise specified.

Table 2

Serial A.C. Characteristics Table

		DATA SHEET		
	SYMBOL	MIN	MAX	UNITS
1. SERIAL-IN SET-UP TIME	t_{SPIN}	120		ns
2. CONTROL BUS SET-UP TIME	t_{CIN}	180		ns
3. SERIAL OUTPUT ACCESS TIME	t_{ACC}		260	ns
4. ADDRESS SELECT ACCESS TIME	t_{AS}		120	ns
5. ADDRESS DE-SELECT ACCESS TIME	t_{AD}		120	ns

Table 3

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{DD}	-.3 to +12V
STORAGE TEMPERATURE	-25°C to +125°C
LEAD TEMPERATURE (SOLDERING) 10 SEC	+333°C

STANDARD CONDITIONS

V_{DD}	+4.6V to +6.0V
OPERATING TEMPERATURE	0°C to +55°C

SUPPLY CURRENT

I_{DD}	82 ma maximum	V_{DD} = 6.0V V_{SS} = 0.0V

ROM clock frequency typically 1.56MHZ

Table 4

TABLE OF VALID SPB ADDRESSES

VALID SPB ADDRESS (HEX)	AD2	AD1	AD0	FUNCTION READ SPB (DIB)*	WRITE TO SPB (DW:DWS)
0080	1	0	0	Bit 16 outputs condition on LRQ Input	Bus copy SD0-SD7 to D0-D7 (Speech chip start address)
001	1	0	0	Bit 16 outputs full/$\overline{\text{full}}$ flag	Bit 10=0: copies SD0-SD9 on to stack Bit 10=1: clear FIFO array
0082-00FF	1	0	0	*Copies D0-D7 to SD0-SD7	Copies SD0-SD7 to D0-D7
01FE-01FF	1	0	1	*Copies D0-D7 to SD0-S07	Copies SD0-S07 to D0-D7
0700-07FF	1	1	0	*Copies D0-D7 to SD0-S07	Copies SD0-S07 to D0-D7
0800-08FF	0	0	0	*Copies D0-D7 to SD0-S07	Copies SD0-S07 to D0-D7
0900-09FF	0	0	1	*Copies D0-D7 to SD0-S07	Copies SD0-S07 to D0-D7
0A00-0AFF	0	1	0	Copies D0-D7 to SD0-S07	Copies SD0-S07 to D0-D7
0800-08FF	0	1	1	*Copies D0-D7 to SD0-S07	Copies SD0-S07 to D0-D7
Any Other	1	1	1	*Tri-state SD0-SD15	Accept no inputs

*NOTE: Any non-functional SD0 through SD15 is forced to Logic '1' during read. All these valid SPB addresses bus copy the address from SD0-15 to D0-7 during the preceding BAR.

Table 5

SPB-640 C1, C2, C3 CONTROL STATES

C1	C2	C3	Function	
0	0	0	NOP	- No action taken.
0	0	1	ASR Load	- Accepts data from the serial input, synchronous to the externally supplied ROM clock. This data is shifted into the ASR holding register in preparation for loading into the PC. Although ASR is 16 bits long, it is not necessary to load all 16 bits of address sequentially in one ASR load.
0	1	0	PC Load	- Loads the contests of the ASR register into the PC.
0	1	1	DSR Load	- DSR Load puts the SERIAL OUT pin in or out of tristate depending upon the validity of the address in PC. Both these signals are otherwise used to generate 10 bit word DSR Load/DSR Shift cycles internally.
1	0	0	DSR Shift Out	- Shifts data in DSR out synchronous to the RCL.
1	0	1	Load Stack-Subroutine	- Latches the condition of whether the SPB was enabled during the presently executing Jump-cycle executed by the SP-0256.
1	1	0	Return-	- Re-enables the SPB S_{out} upon the execution of an SP-0256 RETURN instruction, if the SPB was enabled before the start of the present SP-0256 executing subroutine.
1	1	1	NOP	- No action taken.
1	0	1	Load Stack	- Latches the condition of the SPB having been enabled during the present sub-routine.
1	1	0	Return	- Re-enables the SPB on the conditon that the "Load Stack" latch is set.